1 **REMARKS**

2 The Applicants respectfully request reconsideration and allowance of claims 1-18 in view

3 of the following arguments.

4

5 <u>INTERVIEW SUMMARY</u>

6 The Applicants appreciate the telephone interview conducted on October 6, 2005,

7 between Examiner Tat and the undersigned attorney. In the interview, the undersigned attorney

8 summarized the arguments presented below, in particular, emphasizing the distinctions between

9 the logic circuit design method disclosed in U.S. Patent No. 6,460,166 to Reddy et al. ("Reddy"

10 or the "Reddy patent") and the logic circuit design method required in the claims of the present

11 application. No agreement was reached as to the allowability of the claims. Additionally, the

12 Applicants' appreciate the indication by the Examiner in the interview that the objections to

13 claims 1 through 18 will be withdrawn.

14

15 <u>STATUS OF THE CLAIMS</u>

16 The present application was filed with claims 1 through 18. None of the claims have

17 been amended. Claims 1 through 18 remain pending in the case.

18

19 <u>CLAIMS 1-18 ARE NOT ANTICIPATED BY THE REDDY PATENT</u>

20 The current Office Action rejects claims 1 through 18 under 35 U.S.C. § 102(e) as being

21 anticipated by the Reddy patent. The Applicants respectfully traverse these rejections.

22

23

1   <u>Independent Claim 1</u>

2   Claim 1 is directed to a method of designing a logic circuit to provide a predetermined

3   logical operation and requires the following elements:

4   (a)   defining a logic synthesis block comprising a dynamic logic circuit;
5   (b)   performing logic synthesis for the predetermined logical operation to produce an
6   intermediate circuit, the logic synthesis being performed utilizing a synthesis
7   library constrained to the logic synthesis block;
8   (c)   eliminating unused devices in the intermediate circuit to produce a final circuit;
9   and
10   (d)   sizing the devices in the final circuit.
11

12   The current Office Action attempts to equate each of the above elements of claim 1 with

13   some aspect disclosed in Reddy by citing the language of Reddy from col. 4, line 23 through col.

14   7, line 55. In particular, Reddy describes a design automation system that has libraries for use in

15   building circuits (Reddy at col. 4, lines 27-29). The libraries have "books" or "cells" of pre-

16   designed circuits for performing certain Boolean functions, such as AO and OA books (Reddy at

17   col. 4, lines 23-26). In addition, the different books are weighted differently based on a cost

18   function where the cost function may include criteria, such as transmission delay, area, and

19   manufacturing costs (Reddy at col. 6, lines 17-21). Reddy discloses that circuitry may be

20   restructured by converting certain specified logic blocks in the circuitry to a particular logic

21   pattern from the library (Reddy at col. 4, lines 29-31). The restructuring process includes

22   compiling a list of books for all of the transformations that may be performed on the circuit based

23   on the matches between the books in the library and the logic blocks in the circuit (Reddy at col.

24   6, lines 43-47). The list is sorted by benefit according to the respective cost functions for each

25   book (Reddy at col. 6, lines 47-52). If multiple books are matched with a particular logic block,

26   then the redundant books are eliminated and the pattern with the better benefit is retained (Reddy

27   at col. 6, lines 50-52).

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1   The Applicants respectfully submit that Reddy fails to disclose several of the limitations

2   required by Applicants' claim 1. Specifically, Reddy does not disclose performing logic

3   synthesis for a predetermined logical operation to produce an intermediate circuit where the logic

4   synthesis is performed using a synthesis library constrained to a particular logic synthesis block,

5   as required by element (b) of claim 1. Additionally, Reddy does not teach or suggest eliminating

6   unused devices in the intermediate circuit to produce a final circuit nor, sizing the devices in the

7   final circuit, as required by elements (c) and (d) of claim 1, respectively.

8   Because Reddy does not disclose all of the limitations required by claim 1, claim 1 cannot

9   be anticipated by the Reddy patent. Therefore, the Applicants assert that claim 1 is in condition

10   for allowance along with its respective dependent claims, claims 2 through 7.

11

12   Independent Claim 8

13   Claim 8 is directed to a method of synthesizing a logic circuit to provide a predetermined

14   logical operation. This claim requires some of the limitations required by claim 1. In particular,

15   claim 8 requires performing logic synthesis for the predetermined logical operation to produce an

16   intermediate circuit where the logic synthesis uses a synthesis library constrained to a dynamic

17   logic circuit that includes only a particular logic synthesis block. As discussed above with

18   respect to claim 1, Reddy does not disclose this limitation. Therefore, since Reddy does not

19   disclose all of the limitations required by claim 8, claim 8 cannot be anticipated by the Reddy

20   patent.

21   For these reasons, the Applicants assert that claim 8 is in condition for allowance along

22   with its respective dependent claims, claims 9 through 12.

1   Independent Claim 13

2   Independent claim 13 is written in a form that complies with 37 C.F.R. §1.75(e). The

3   preamble of a claim under 37 C.F.R. §1.75(e) comprises a general description of the steps in the

4   method that are conventional or known. The preamble is followed by the proposed

5   improvements.

6   The preamble of claim 13 is directed to a circuit design method utilizing a logic synthesis

7   tool and predefined logic circuit library to provide a logic implementation for a predetermined

8   logical operation. The improvements required by claim 13 are similar to some of the limitations

9   required by independent claim 1. In particular, claim 13 requires constraining the logic synthesis

10   tool to a particular logic synthesis block. As discussed above with respect to claim 1, Reddy

11   does not disclose this limitation. Therefore, since Reddy does not disclose all of the limitations

12   required by claim 13, claim 13 cannot be anticipated by the Reddy patent.

13   For these reasons, the Applicants assert that claim 13 is in condition for allowance along

14   with its respective dependent claims, claims 14 through 18.

1   <u>CONCLUSION</u>

2   For all of the above reasons, the Applicants respectfully request reconsideration and

3   allowance of claims 1 through 18.

4   If any issue remains as to the allowability of these claims, or if a conference might

5   expedite allowance of the claims, the Examiner is asked to telephone the undersigned attorney

6   prior to issuing a further action in this case.

7

8   Respectfully submitted,

9   THE CULBERTSON GROUP

10

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22   CERTIFICATE OF FACSIMILE

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24 I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, (Fax No. 571-273-8300) on October 12, 2005.

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